

A MODIFIED ARCHITECTURE OF MULTIPLIER AND ACCUMULATOR USING SPURIOUS POWER SUPPRESSION TECHNIQUE

R.Mohanapriya^{#1}, K. Rajesh^{*2}

[#] PG Scholar (VLSI Design), Knowledge Institute of Technology, Salem

^{*} Assistant Professor, Department of ECE, Knowledge Institute of Tehnology, Salem

mohanapriya488@gmail.com
krece@kiot.ac.in

Abstract---High speed and low power Multiplier and Accumulator (MAC) unit is at most requirement of today's VLSI systems and digital signal processing (DSP) applications like FFT, Finite Impulse response filters, convolution etc. In this modified architecture, Radix-4 Modified Booth Encoding (MBE) is used to produce the partial products. In this multiplication and accumulation has been combined using a hybrid type of Carry Save Adder (CSA). So the performance will be improved. A Carry Look ahead Adder is inserted in the CSA tree to reduce the number of bits in the final adder. In booth multiplication, when two numbers are multiplied some portion of the data may be zero. By neglecting those data, power has been reduced. For this purpose Spurious Power Suppression Technique (SPST) is used to remove useless portion of the data in addition process. In this modified architecture, the overall process is three stages to produce the result. The modified MAC operation is coded with Verilog and simulated using Xilinx 12.1.

Keywords---DSP, MAC, Radix-4, Modified Booth Encoding, CSA, CLA, SPST, Verilog.

I. INTRODUCTION

For Digital Signal Processing (DSP) like Fast Fourier Transform (FFT), Finite Impulse Response (FIR) filters, convolution etc... required high speed and low power MAC. The multiplier and Multiplier and Accumulator (MAC) [1] are the important blocks of the processor and have a great impact on the speed of the processor.

MAC is the necessary element of the digital processing system such as filtering, convolution and inner products. Many researchers are designing MAC for high performance and low power consumption. An efficient multiplier should have following characteristics: Accuracy- A good multiplier should give correct result, Speed-Multiplier should perform operation at high speed. Area-multiplier should occupy less number of slices and LUT's, Power-Multiplier should consume less power. Basically Multiplier consists of three

basic steps: Booth Encoding, Partial product generation and final addition. For MAC additionally accumulator used.

Modified Booth Algorithm (MBA) [4] is the method commonly used for achieving high speed multiplication and also reduce number of partial products. Also by using radix-4, radix-8, radix-16 and radix-32 booth Encoding technique, the partial products are further reduced, which increases complexity and improves the performance [1]. Also by using MBA algorithm speed, has been increased. For this purpose many parallel multiplication have been analyzed. [2]-[4].

Elguibaly [5], proposed one of the advanced types of MAC for general-purpose digital signal processing. In this hybrid type of Carry Save Adder has been used for combining the partial product summation with accumulation. This CSA tree compresses partial products with accumulation process. In this adder for accumulation process was eliminated.

In this paper, a new architecture for a high-speed MAC is proposed. The most effective way to increase the speed of a multiplier is to reduce the number of the partial products by Radix-4 modified booth multiplier. In this MAC, the computations of multiplication and accumulation are combined and a hybrid-type CSA structure is proposed to reduce the critical path and improve the output rate.

Increasing the operands density is important aspect. This has been done with the help of a modified array structure. In this modified architecture a hybrid type of CSA is used. This CSA contains the Carry Look ahead Adder, Full Adder and Half Adder. Also Intermediate calculation results are accumulated in the form of sum and carry instead of the final adder outputs.

Then Spurious Power Suppression Technique has been used to achieve less power consumption. Whenever two numbers are multiplied, some of the rows will be zero. By neglecting those data power has been reduced.

II. OVERVIEW OF MAC UNIT

In digital signal processing, the basic operation is multiplication and accumulation. The MAC unit provides the

operations such as high speed multiplication, multiplication with cumulative addition and subtraction, saturation, clear operations. Hence, If a MAC is working under high speed operation, it can be able to support multiple operations and parallel

MAC is comprises of three important sections:

1. Adder,
2. Multiplier
3. Accumulator.

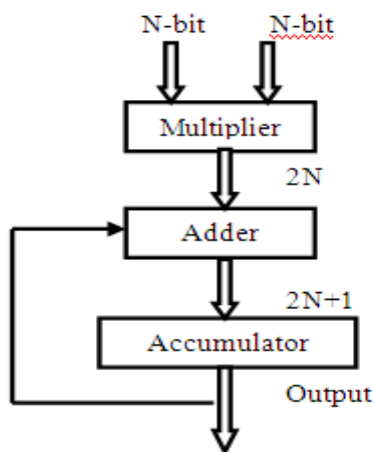


Fig: 1 Basic MAC unit

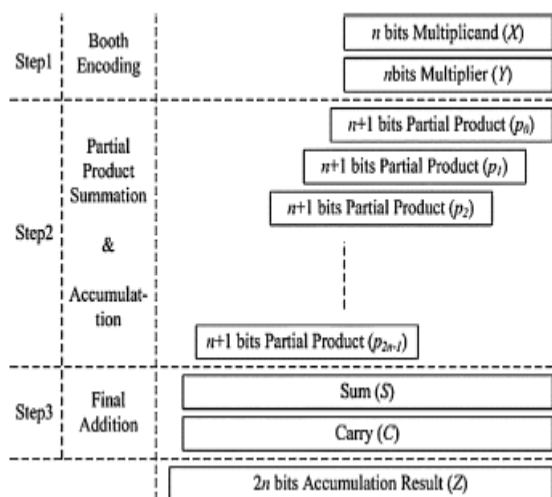


Fig:2 Basic arithmetic steps of multiplication and accumulation (3 stages)

If an operation to multiply two N-bit numbers and accumulates into a 2N-bit number is considered, the critical path is determined by the 2N-bit accumulation operation. Since accumulation is carried out using the result

from step 2 instead of that from step 3, step 3 does not have to be run until the point at which the result for the final accumulation is needed.

III. PROPOSED MAC ARCHITECTURE

In this modified architecture, Radix-4 Modified Booth Encoding (MBE) is used to produce the partial products. In booth multiplication, when two numbers are multiplied some portion of the data may be zero. By neglecting those data, power has been reduced. For this purpose Spurious Power Suppression Technique (SPST) is used to remove ineffective portion of the data in addition process. In this modified architecture the accumulation is carried out along with partial product summation. So that number of stages will get reduced. Multiplier (N bits) and multiplicand (N bits) will be given to the Radix-4 Modified Booth Encoder. To multiply multiplier and multiplicand Radix-4 booth algorithm starts from grouping multiplicand by three bits and encoding them into one of (-2, -2, 0, 1, 2). (i.e). Then these three bits will be converted into single bit. Here 4 rows of partial products will be generated.

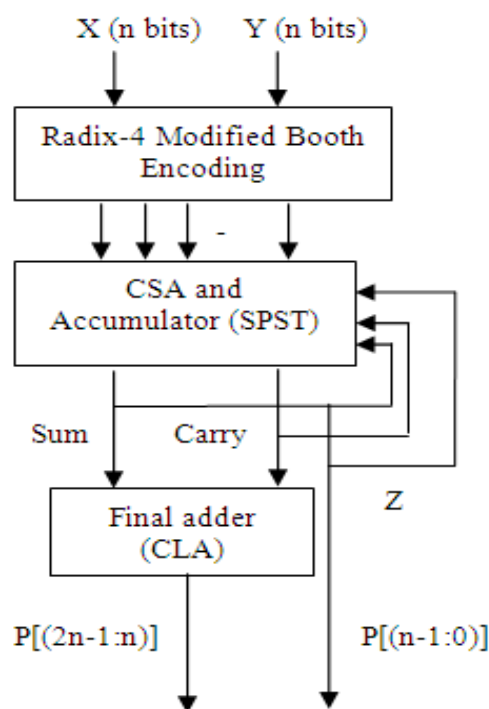


Fig: 3 Architecture of Proposed MAC

By using Spurious Power Suppression Technique (SPST) ineffective portion of the data is removed for reducing the power consumption. This technique is controlled by detection unit. The detection unit has one of the operands as its input to check unwanted portion.

Steps:

1. Radix-4 Modified Booth Encoder
2. CSA and Accumulator
3. Final addition

If the accumulator has been eliminated, the critical path is then determined by the final adder in the multiplier. The basic method to improve the performance of the final adder is to decrease the number of input bits. In order to reduce this number of input bits, the multiple partial products are compressed into a sum and a carry by CSA. A 2-bit CLA is used to add the lower bits in the CSA. In addition, to increase the output rate when pipelining is applied, the sums and carries from the CSA are accumulated instead of the outputs from the final adder in the manner that the sum and carry from the CSA in the previous cycle are inputted to CSA.

IV. RADIX-4 BOOTH ENCODING

Booth multiplication is a technique that allows for smaller, faster multiplication circuits, by recoding the numbers that are multiplied. It is possible to reduce the number of partial products by half, by using the technique of radix-4 Booth recoding.

The basic idea is that, instead of shifting and adding for every column of the multiplier term and multiplying by 1 or 0, we only take every second column, and multiply by ± 1 , ± 2 , or 0, to obtain the same results. The advantage of this method is the halving of the number of partial products. To Booth recode the multiplier term, we consider the bits in blocks of three, such that each block overlaps the previous block by one bit.

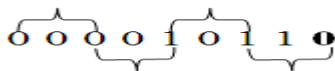


Fig 4: Grouping of bits from the multiplier term

Table 1: Radix-4 Booth Recoding

Block	Recoded Digit	Operation on X
000	0	0
001	+1	+1
010	+1	+1
011	+2	+2
100	-2	-2
101	-1	-1
110	-1	-1
111	0	0

Grouping starts from the LSB, and the first block only uses two bits of the multiplier. Figure 4 shows the grouping of bits from the multiplier term for use in modified booth encoding. Each block is decoded to generate the correct partial product. The encoding of the multiplier Y, using the modified booth algorithm, generates the following five signed digits, -2, -1, 0, +1, +2. Each encoded digit in the multiplier performs a certain operation on the multiplicand, X, as illustrated in Table 1.

V. SPURIOUS POWER SUPPRESSION TECHNIQUE

The SPST technique is basically depend on the radix 4 modified booth algorithm. It deals with the recoding of the given multiplicand and reduces the number of the intermediate stages in the multiplication operation which maintains the speed of the process at the same time the power consumed will be reduced. The SPST uses a detection logic circuit to detect the effective data range of arithmetic units, e.g., adders or multipliers. When a portion of data does not affect the final computing results, the data controlling circuits of the SPST latch this portion to avoid useless data transitions occurring inside the arithmetic units.

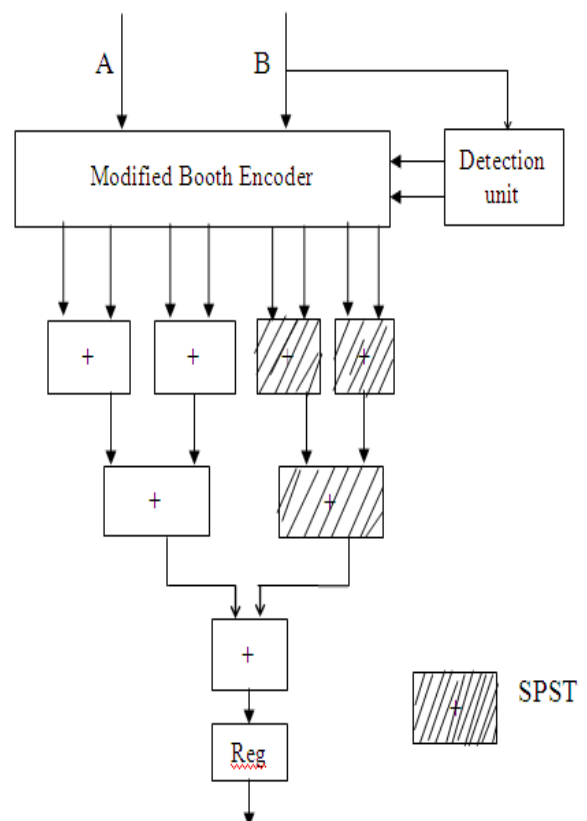


Fig:5 Spurious power suppression technique

VI. CSA ARCHITECTURE

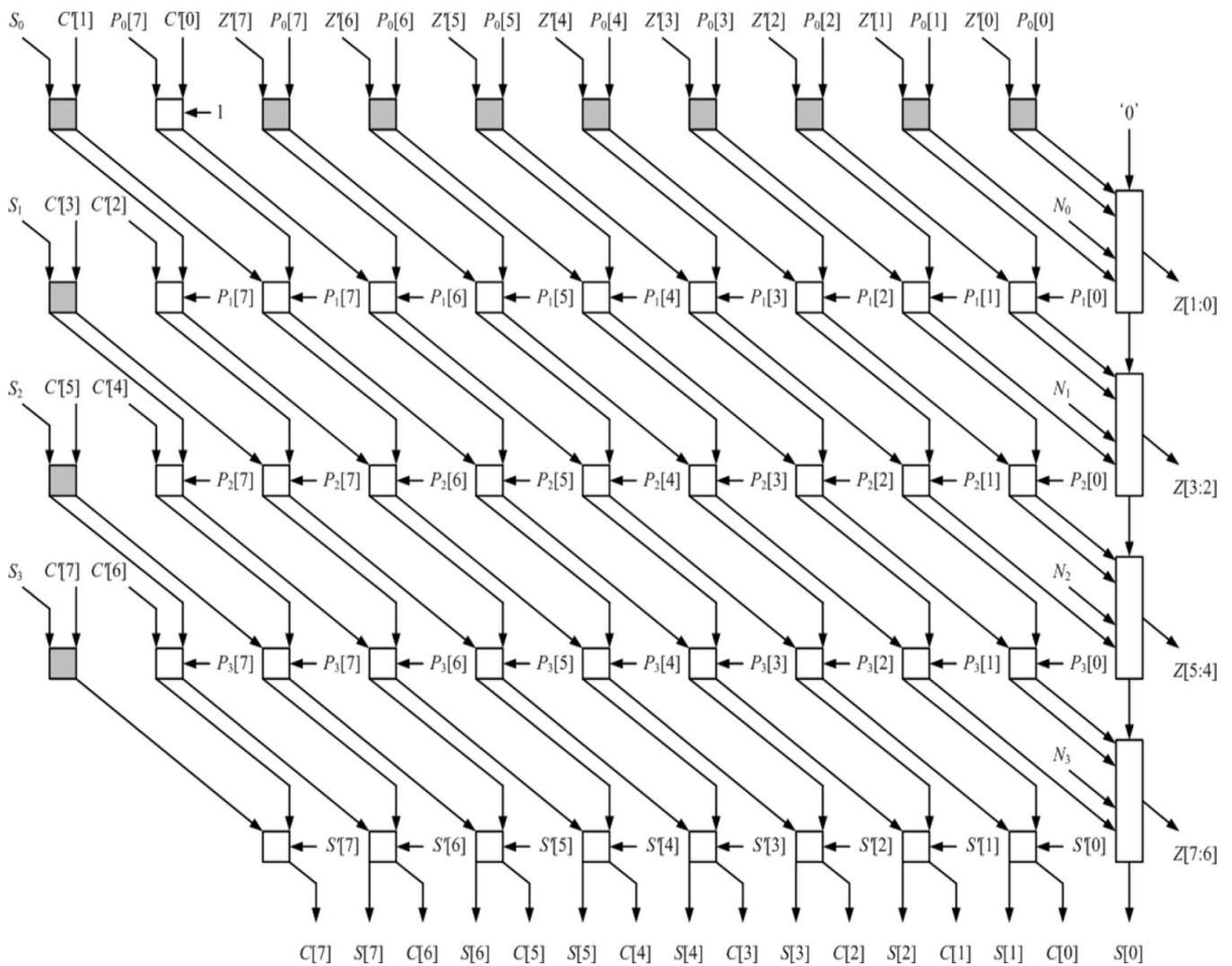


Fig 6:CSA and Accumulator architecture

Hybrid type of CSA architecture works with the help of proposed MAC is shown in Fig.6. It performs 8*8 operation (i.e) 8 bit operation. In that architecture, N_i is used to compensate 1's complement number. Then S_i is used to simplify the sign extension. From Booth encoder partial products are generated. Partial products are $P_0 [7:0]$, $P_1 [7:0]$, $P_2 [7:0]$, $P_3 [7:0]$. Only four rows of partial products generated instead of eight rows. By using this architecture, five FA adder rows needed. One more row is for accumulation process.

For any $N*N$ bit operation, the total number of CSA is $(n/2+1)$ levels. In fig.6, for Full Adder operation, White Square

box is used, the gray square box is used for Half Adder operation and rectangular symbol is used for 2 bit carry Look ahead Adder operation. This CLA contains five inputs with carry input.

VII.FINAL ADDER

This stage is also crucial for any MAC because in this stage addition of large size operands is performed so in this stage fast carry propagate adders like Carry-look Ahead Adder or Carry Skip Adder or Carry Select Adder and other adders such as Carry Save Adder can be used as per requirement. But analyzing all the adders, Carry Look ahead Adder gives low power and speed of

operation. Also it provides least area-delay product. This adder ~~ignends~~ and addend if a higher order carry is generated. based on the principle of looking at the lower order bits of the

VIII.RESULTS AND DISCUSSION

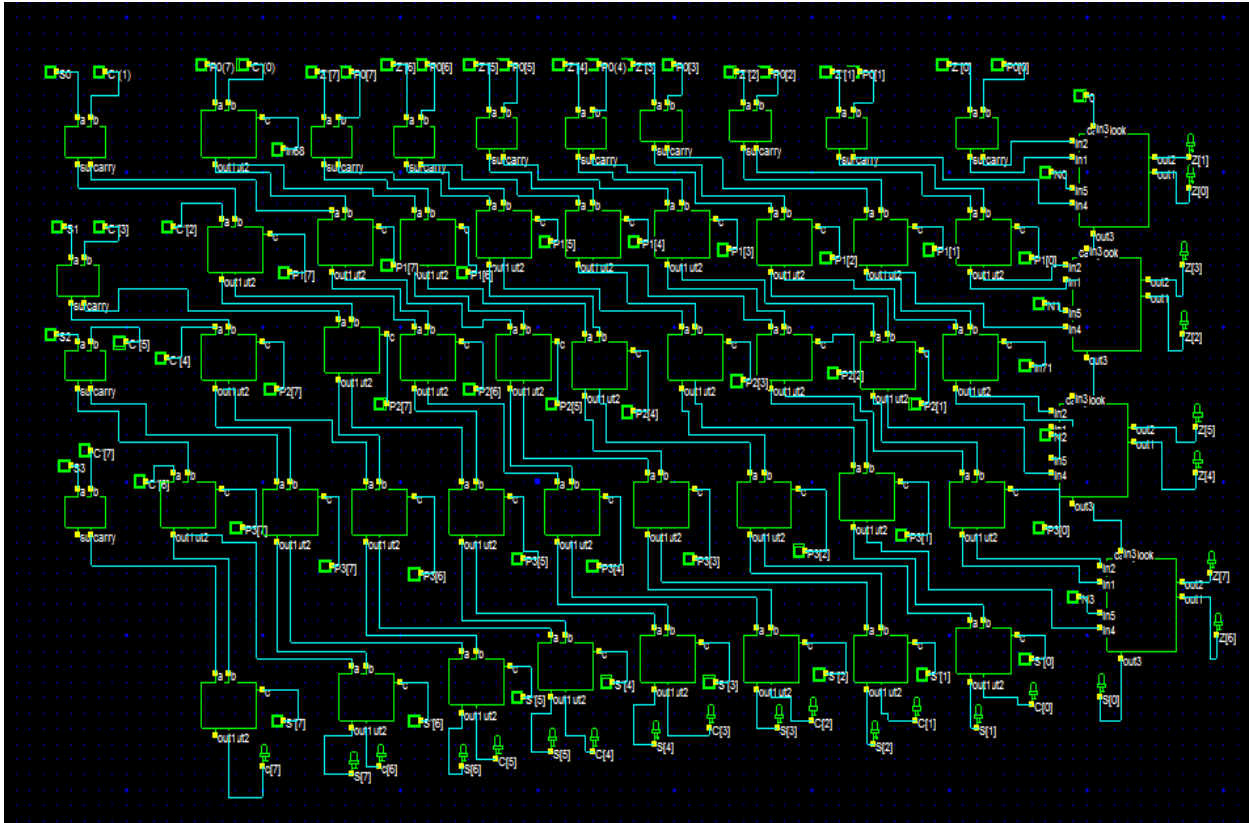


Fig 7: Architecture of CSA using Microwind tool

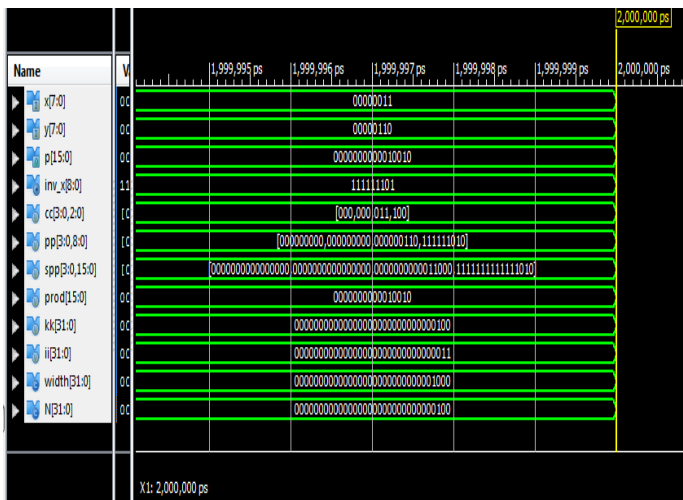


Fig: 8 Simulation Results for 8*8 Booth multiplier

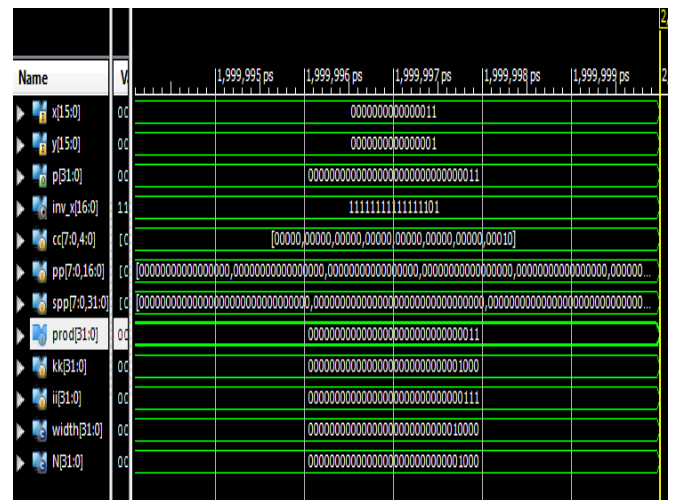


Fig: 9 Simulation Results for 16*16 Booth multiplier

In figure 7, the architecture of (8*8) multiplication and accumulation has been performed using Microwind tool. By using Radix-4 Booth algorithm the partial products are generated. In this architecture half adders, full Adders and Carry look ahead adders are used for addition process. By passing partial products into the adder blocks 16 bit MAC output has been obtained.

The simulation results for 8-bit and 16-bit booth multiplier using Radix-4 Modified Booth algorithm shown in figure 8 and 9. By using Radix-4 Booth algorithm the partial products are reduced by n/2.

From figure 8, 4 rows of partial products only produced. From figure 9, 8 rows of partial products only produced. Also delay has been analyzed. Then these partial products are added and produced the 16 bit and 32 bit multiplied output. From figure 8 to 9, results have been obtained with the help of Xilinx 12.1 ISE design suite.

Table 2: Delay analysis

8*8 Booth Multiplier	16.234 ns
16*16 Booth Multiplier	23.610 ns

IX. CONCLUSION

Higher radix MBA and partial reduction technique gives good result in terms of speed as well as area. Radix-4 modified booth algorithm reduces the number of partial products, which improves the speed. By removing independent accumulation process that has the largest delay and merging it to the compression process of the partial products, the overall MAC performance has been improved. Also by using Spurious Power Suppression Technique, power has been reduced by eliminating ineffective portion of data.

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ABOUT THE AUTHORS



R. Mohanapriya is currently pursuing her M.E degree in VLSI Design from Anna University, Chennai in Knowledge Institute of Technology, Salem. She has received her B.E degree in Electronica and Communication from Anna University, Chennai in Gnanamani college of Technology, Namakkal. She is a member in IEEE.



K. Rajesh, Assistant Professor in the Department of ECE in Knowledge Institute of Technology, Salem. He received received his B.E (ECE) in Sona College of Technology, Salem and M.E (VLSI Design) in Bannari Amman Institute of Technology, Sathyamangalam. Research interest in device modeling in VLSI, Anolgd design. He is a member in IEEE.