



CENSORSHIP OF LEAKAGE PARAMETERS OF A FINFET BASED SCHMITT TRIGGER AT NANO-METER REGIME

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Abstract

Purpose: Recently FinFET technology has gained a lot of attention because of its superior fabrication process that is very similar to the fabrication of a conventional transistor. FinFETs unique feature as well as the potential applications make it a strong contender for the low power chip designs. Research is in full swing to use FinFET in analog circuits like Schmitt trigger, sensors, OPAMP and digital logic. The realization of the FinFET based circuits predicts that it is possible to broaden the concept of Moore's law without unstoppable scaling of CMOS devices.

Methodology: This work is carried out on the Cadence Simulation tool. After the simulation, all these parameters have been compared with previous published 4T Schmitt trigger at 45nm with this design and found that they are in close vicinity.

Main Findings: By combining the superior flexibility and reduced short channel effects (SCEs) of FinFET devices offers a promising approach to implement highly integrated, power-efficient Schmitt Trigger circuit for low power digital applications. Schmitt trigger is a device capable of removing unwanted noise from the input and prevent the other operations from this unwanted noise and improve the performance of the device.

Implications: This study is discussing and performs a comparative analysis of different leakage parameters of a FinFET based Schmitt Trigger with previous 4T Schmitt Trigger at 45nm.

The novelty of Study: Size, power, speed, Cost etc. are important factors for designing any new circuits in the field of Electronics. Various eminent researchers have been making efforts for this. This paper makes some effort to discuss about past research and design a new circuit where the value of delay, leakage power and dynamic power reduces when compared to previously published circuits.

Keywords: Schmitt Trigger, Slew Rate, Leakage Power, Average Power, Delay.

INTRODUCTION

The optimization of power has become very necessary due to the increased number of transistors per unit area and the higher portability demands of the user. Power Dissipation in VLSI circuits is mainly arisen due to three major sources: power required to charge or discharge a node, power due to the output transition and power due to leakage current. Various techniques were devised by the designers for the minimization of power in circuits. Sleep Transistor approach, Multi-Threshold CMOS, SVL, AVL and Hybrid techniques are remarkable for the reduction of leakage currents, which constitutes a major fraction of power in the nano-regime (Steyaert, M. & Sansen, W. (1986)). The sizing of the transistor is also helpful for minimizing power. By lowering the supply voltages (voltage scaling), power can be saved but the system works slower. In 1965 Gordon Moore published a chapter that expresses the brightest future of integrated technology. Only after 6 years, first monolithic IC was invented, As Moore already mention that IC technology evolves the cost of the transistor decreases steadily that means that a large number of the transistor are going to fitted onto a single silicon chip. Short channel devices are those devices which use the transistors with channel lengths less than 3 to 5micron. Short channel devices comprehensively reduce the ratio between lateral and vertical dimensions (Pfister, A. (1992)). The effects of the transition region from the drain the source diffusions to the channel become significant, causing the need for increased complexity in the device model. The rest of the manuscript is arranged as given. In section II, presents about the description of Schmitt trigger and their characteristics with simulation results. Finally, the conclusion and directions for the future scope of research are given in Section III.

SCHMITT TRIGGER

Traditional Schmitt Trigger is configured which is an operational amplifier along with resistance where it forms a positive feedback network that the reason traditional Schmitt Trigger design is suited for the complementary-MOS technology implementation, due to the presence of feedback, circuit output accuracy is weakened, makes wastage of die area and give a small amount of sheet resistance. This is the reason where various conventional CMOS designed Schmitt trigger circuits have emerges in a few years. Traditional Schmitt Triggers have large gain for an operational amplifier so it consumes many areas of the chip (Wang, Z. (1991)). MOSFET from the last few years scaled-down largely which is giving birth to the short channel effect. IC performance now depends on the dimensions of the scaling factor so the improvement of such force is important. Figure 1 is a diagram of high-speed Schmitt trigger with 5 transistors.

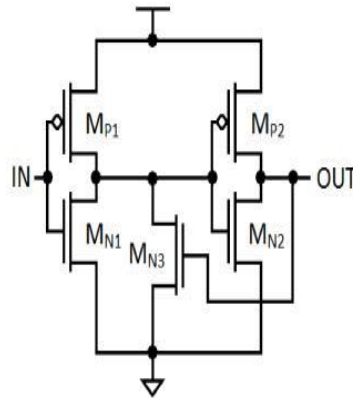


Figure 1: 5T high speed Schmitt Trigger

Now as we scaled down the channel length of the MOSFET some major concerns are arising such as velocity saturation, gate leakage, short channel effects, sub-threshold voltage, mobility degradation and leakage current at below 90nm technology. All these reliability problems are overcome in the new device and also in new material as power consumption increases the heat dissipation is also increases so we required the new device and its application which are used in the VLSI circuits. Moore's law is now not applicable because of the fast-developing technology of VLSI design industries so the conventional devices are replaced by the newly discovered devices and the upcoming devices are target to apply Moore's law in the circuit, FinFET is used as a new device which is work below 22nm technology also and its power consumption is also low due to which heat generation is less in the circuit with good mechanical, electrical and thermal properties. FinFET is used in various places such as where we use CMOS now we can use the FinFET circuit it provides great electrical property in the circuit and provides great electrostatic control in the circuit at the gate which provides high driving current (Dokic, B.L. (1984)).

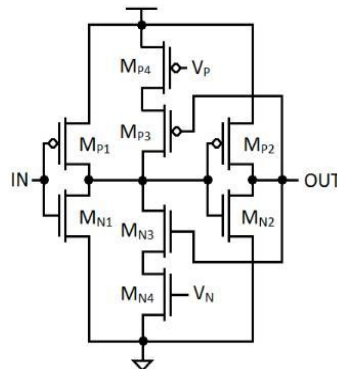


Figure 2: Show the 8T Schmitt trigger

Various complementary-MOS Schmitt Trigger designs have been discovered in the last few years and design is based on the application which we required in the field. Various Schmitt Trigger circuits are studied in the chapter and compared with each other. M_{P1} - M_{N1} and M_{P2} - M_{N2} are the two basic inverters present in the 5T Schmitt Trigger and feedback are provided by the additional nMOS (M_{N3}) transistor as shown in Figure below hysteresis characteristic in the circuit is controlled by the M_{N3} transistor and the width of the hysteresis characteristic is monitored and varied by feedback transistor.

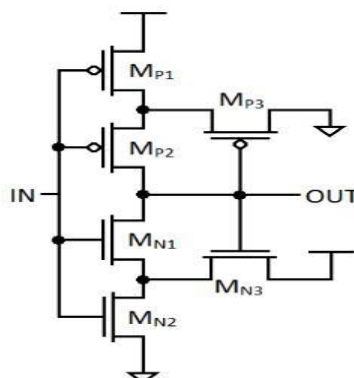


Figure 3: Show the 6T Inverting Conventional Schmitt Trigger

In this design, we get a higher switching speed. nMOS and pMOS are the two inverter amplifiers with one basic inverting amplifier and there are three pairs of inverters that given in figure 3, this comprises the 6T Schmitt trigger. In wireless communication, the main requirement is the low power consumption but 6T Schmitt trigger have four transistors in its so it consumes more power so it is not used in the low power circuit. However, the 4T Schmitt trigger (Weste, N. & Eshraghian, K. (1993)) is designed by using a combination of one pMOS (Pi) and three nMOS (Ni, N2 and N3) at 45nm CMOS technology node, this circuit does not have a direct connection from voltage supply to the ground node. Hence it provides the advantage of no static power dissipation. Table 1 describes the parameter like leakage power and delay of the 4T Schmitt trigger. In this Schmitt trigger the hysteresis characteristics control by the electrically controlled signal know as V_P and V_N that permit the hysteresis of the circuit is controlled by the signals which is the use of off-chip potentiometers. As M_{P3} - M_{P4} and M_{N3} - M_{N4} transistor resistor of the circuit is varied with V_P and V_N of the circuit respectively (Pedroni, V. A. (2005)).

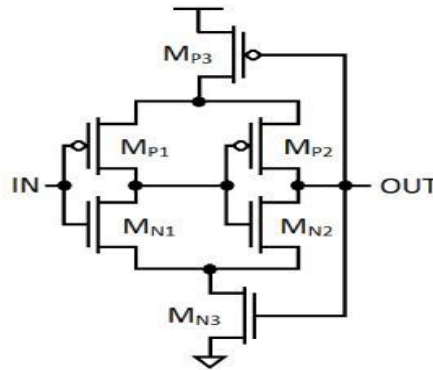


Figure 4: 6T low power Schmitt trigger

In this process, the threshold voltage of the circuit is adjusted. Due to this process, the static power dissipation of the circuit is decreased. Different characteristics and their results are described below.

a. Slew rate

The design of the N-type and P-type transistor very crucial because due it there is a short time when both P-type and N-type transistor is switch on at the same time at the transition of either 0 to 1 or 1 to 0, this gives the current short pulse from to V_{ss} for a very short time (Saxena, A. et al., (2014)).

Table 1: Slew rate of the FinFET based Schmitt trigger

V_{dd} (volts)	Slew Rate (volts/pSec)
0.6	5.88
0.7	6.864
0.8	4.978
0.9	3.727

From table 1, we can observe that it achieves a maximum slew rate of 6.864 volts/psec for a time 269.6 pSec at 0.7 volts. Hence at 0.7volts change its output rapidly.

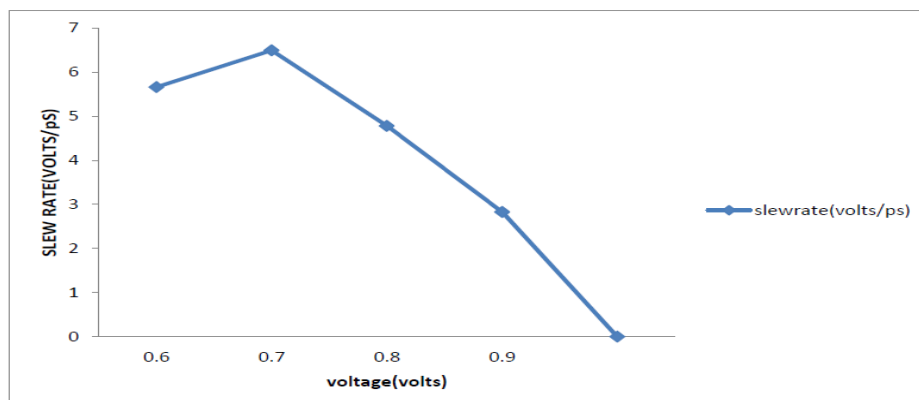


Figure 5: Shows the Slew Rate of 4T Schmitt Trigger

Figure 5 elaborates that there is a reduction in delay of FinFET based Schmitt trigger 37.38% at 0.7 volts power supply from 4T Schmitt trigger.

Table 2: 4T Schmitt trigger parameters

Supply Voltage	Leakage power(pW)	Delay(pSec)
0.6	2.54	540.3
0.7	4.86	485.4
0.8	13.98	409.78
0.9	14.34	389.29

Table 2 describes the characteristics i.e. leakage power and delay of 4T Schmitt trigger at different voltages. In this Schmitt trigger we allowing the B_p and B_n that is trans-conductance parameters are same then the width of the hysteresis (Mishra, V. & Akashe, S. (2015)) of the circuit becomes independent of the threshold voltage and now the hysteresis is depended the only o the supply voltage and the geometry of the circuit. In the 6T low power Schmitt trigger, there are three transistors incorporated with the CMOS design as shown in figure 6.

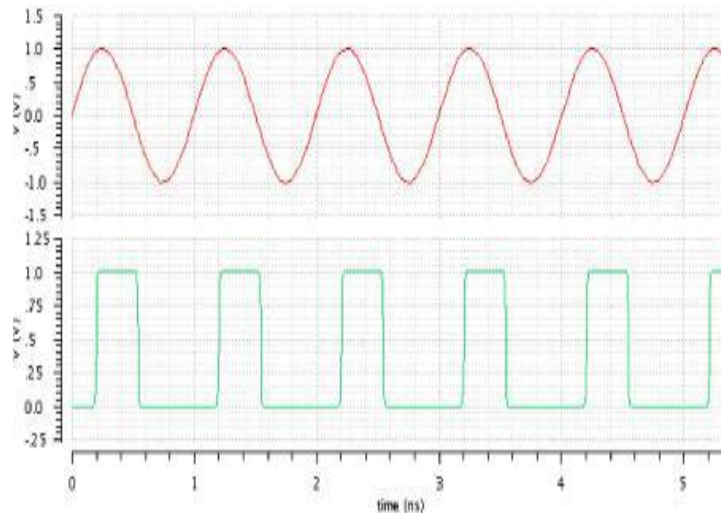


Figure 6: FinFET Schmitt trigger input-output waveform

b. Delay

Delay is termed as the fifty percent input and fifty percent of output time taken by the signal is called the delay of the circuit. Delay can be also termed as the time required by the signal to propagate from input to output node (Mishra, V. & Akashe, S. (2014)).

$$\text{Delay} = 0.69 R_{eq} \times CL \quad (1)$$

Where equivalent resistance of the design is given by R_{eq} and the load capacitance is given by CL. FinFET based Schmitt trigger reduces the delay by 21.26% at 0.7volts power supply from 4T Schmitt trigger (Al-Sarawi, S. F. (2002)).

c. Power analyses

The energy consumption per unit time is known as the amount of power dissipated in the circuit. Charging and discharging of the load capacitor gives rise to the dynamic power dissipation. The transient switching current is also coming in the picture in this charging and discharging of the capacitor (Khandelwal, S. et al., (2013)). The design of the N-type and P-type transistor very crucial because due it there is a short time when both P-type and N-type transistor is switch on at the same time at the transition of either 0 to 1 or 1 to 0, this gives the current short pulse from V_{dd} to V_{ss} for a very short time.

d. Dynamic & leakage power of schmitt

The energy consumption per unit time is known as the amount of power dissipated in the circuit. Charging and discharging of the load capacitor gives rise to the dynamic power dissipation (Katyal, V. et al., (2008)). The transient switching current is also come in the picture in this charging and discharging of the capacitor. The design of the N-type

and P-type transistor very crucial because due it there is a short time when both P-type and N-type transistor is switch on at the same time at the transition of either 0 to 1 or 1 to 0, this gives the current short pulse from V_{dd} to V_{ss} for a very short time (Saini, S. et al., (2009)). Table 3 shows the Average Power and Leakage Power of 4T Schmitt Trigger.

Table 3: Shows the Average Power and Leakage Power of 4T Schmitt Trigger

V_{dd} (volts)	0.6	0.7	0.8	0.9
Average power(pW)	6.45	10.258	1.3458	17.236
Leakage Power(pW)	2.256	2.359	2.456	3.001

CONCLUSION

FinFETs unique feature as well as the potential applications make it a strong contender for the low power chip designs. Research is in full swing to use FinFET in analog circuits like Schmitt trigger, sensors, OPssAMP and digital logic. The realization of the FinFET based circuits predicts that it is possible to broaden the concept of Moore's law without unstoppable scaling of CMOS devices. By combining the superior flexibility and reduced short channel effects (SCEs) of FinFET devices offers a promising approach to implement highly integrated, power-efficient Schmitt Trigger circuit for low power digital applications. After the simulation, all these parameters have been compared with previous published 4T Schmitt trigger at 45nm with this design and found that they are in close vicinity. Our design reduces delay, leakage power and dynamic power.

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