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Optimized Mac Unit

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***Abstract*—In this paper, a new multiplier design is proposed which reduces the number of partial products by 25%. This multiplier has been used with different adders available in literature to implement multiplier accumulator (MAC) unit and parameters such as propagation delay, power consumed and area occupied have been compared in each case. From the results, Kogg tone adder has been chosen as it provided optimum values of delay and power dissipation. Later, the results obtained have been compared with that of other multipliers and it has been observed that the proposed multiplier has the lowest propagation delay when compared with Array and Booth multipliers.**

Keywords-—MAC Unit, RTL Compiler, Propagation delay, multiplier

I. Introduction

In modern computing, specifically in digital signal processing and image processing, most complex operations involve a multiply-accumulate operation, usually performed by a module known as multiply

Accumulate (MAC) Unit. MAC Unit is a fundamental module found in almost every processor available today. MAC Unit finds the product of two numbers, may or may not be floating point numbers, and stores it in a register. Rounding off decimals to required precision is usually done in the case of floating point numbers. In addition to processors, these MAC Units are also found in FPGAs and certain PLCs. MAC Unit is one of the slowest modules present in the processors. So, in order to improve the speed of MAC Unit, and in turn that of the processor, a lot of research is being undertaken to improve the design of these units. Furthermore, with the increased demand for mobile devices, there is also a need to decrease the power consumption and occupied area of the modules.

A typical MAC Unit has three sub units, namely multiplier, adder and accumulator register.

Multiplier finds the various partial products involved. Adder adds up the values of those partial products generated and saves them in the accumulator register. A variety of designs for multipliers and adders have been proposed in the past to improve one or more of the parameters discussed above. In this paper, a new design for multiplier is proposed which when used generates lesser number of partial products when compared to

Traditional multipliers, this multiplier is implemented alongside a famous type of parallel prefix adder known as kogge-Stone Adder and the latency, area and power consumption of the module are analyzed.

II. Proposed Multiplier

A. *Multiplier Design*

Through careful rearrangement of terms the four partial products can be converted to just three with the addition of few gates. For the case of 4 x 4 bit multiplier, with the addition of four gates (two AND and two XOR), the number of partial products can be reduced from four to three (reduction by 25%), as shown in Fig 1.1 b. This has resulted in saving a whole Adder block which reduces complexity of circuit, time taken to compute the product as well power consumed by the circuit.

B. *Simulation Parameters*

In this work, various types of MAC are designed in Verilog and then are synthesized using a Cadence EDA tool called RTL Complier. RTL Compiler, with necessary constraints, also gives other vital information like Propagation Delay (PD), Area occupied (in terms of unit cell area) by the circuit and Power consumed by the circuit (in mW). The code is synthesized using Standard Cell Libraries developed by researchers in Oklahama State University that is in accordance to TSMC's 180 nm processes. 1 V input is used as the power supply VDD.

III. RESULTS AND COMPARISON

Results of 8 x 8 bit proposed multiplier with different adders

Thus the proposed multiplier has been implemented with different types of adders reported in the literature so far and the parameters such as time delay, power of design, Kogge Stone Adder would be the best choice. If power dissipation is the major concern, carry skip adder would be the best one to choose. However, if one needs an adder that has the lowest delay and comparatively lower power dissipation, then Kogge Stone Adder would be the wisest choice as its delay is only 2.342 ns and power dissipation is 1.934 mW. Kogge Stone adder would be the default adder design used henceforth in this paper researchers in Oklahama State University that is in accordance to TSMC's 180 nm processes. 1 V input is used as the power supply V_{DD}.

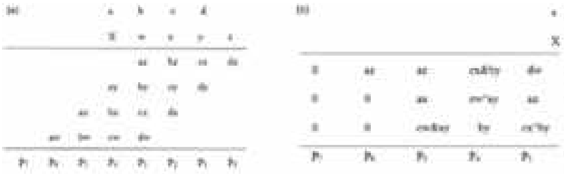

Fig. 1 Multipliers designs (a) Array Multiplier
(b) Proposed Multiplier

Dissipation and area occupied in each case has been computed and are presented in Tables 1.1. The adder types used include Carry Look Ahead adder, Conditional Sum Adder, and parallel prefix adders like Han Carlson adder, Brent Kung adder, Kogge Stone adder and Ladner Fischer Adder [1][2][3]. It can be observed from these data that if the speed of operation of the circuit is the primary objective

C. Comparison with Other Multiplier Types

Simulation results for various 8x8 wide MAC units have been tabulated in table 2. As said above all these units have Kogge stone adder as the adder unit. It can be noticed that the proposed multiplier design is much faster than other popular multiplier designs like Array multiplier and Booth multiplier [4] (16.8% and 11.01% improvement in speed respectively)

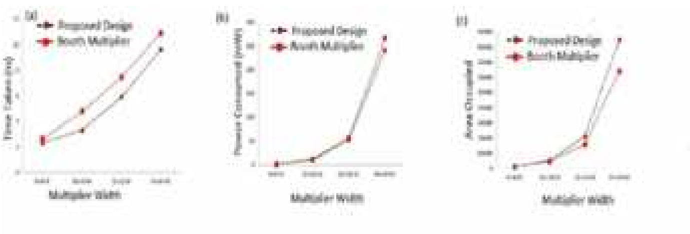

Fig. 2 Comparison of simulation results of increasing multiplier widths between proposed design and Booth multiplier based design.
(a) Propagation Delay. (b) Power Consumption. (c) Area Occupied

TABLE I
Simulation results of 8 x 8 bit design of proposed multiplier

Design	Propa-gation	Power Consumed	Area
	Delay (ns)	(mW)	Occupied
Proposed Design with			
HanCarlson Adder	2.478	1.790	12675
Proposed Design with			
BrentKung Adder	2.517	1.955	12435
Proposed Design with			
KoggeStone Adder	2.342	1.934	13555
Proposed Design with			
LadnerFischer Adder	2.377	1.805	12835
Proposed Design with			
Carry Look Ahead Adder	2.908	1.577	11307
Proposed Design with			
Conditional Sum Adder	2.951	1.881	13104
Proposed Design with			
Carry Skip Adder	3.404	1.419	10908

Though, it consumes more power than booth multiplier and occupies larger area, the tradeoff has been done to keep the MAC Unit a fast operating one.

TABLE II
Simulation results of 8 x 8 bit design of various multipliers

	Propagation	Power	
	Delay		Area
Design		Consumed	
	(nSec)		Occupied
		(mW)	
Proposed			
	2.342	1.934	13555
Design			
Array			
	2.816	2.654	22674
Multiplier			
Booth			
	2.632	1.688	12374
Multiplier			

D. Comparison of Simulation Results with Larger Multiplier Widths

Fig 2 illustrates the simulation results of MAC Units as we scale up the multiplier widths. Fig 2(a) demonstrates that as the multiplier width increases the difference in time taken for computation between proposed design and Booth Multiplier also increases. Hence at larger multiplier widths, proposed design provides better efficiency than Booth multiplier based MAC unit. Though for an 8 x 8 bit multiplier, the proposed design consumes more power than Booth multiplier, it can be observed from Fig 2(b) that for higher multiplier widths Booth multiplier consumes more power because of the increasing complexity of booth recoding units. Fig 2(c) shows that the area occupied by the proposed design remains higher than that by Booth multiplier based design even as multiplier width increases.

E. Comparison with Mac Units Propounded by Others

The time taken to compute a result for a 64x

64 bit is 12.8 ns compared to proposed design's 9.662 ns. In another design proposed by Magnus Sjalander from Charlmers University [6], the time taken to compute result for a 16 x 16 multiplier is 7.80 nsecs using a 135 nm process. In addition, the power consumed in that design (5

mW) is more than twice the power consumed in the proposed design.

A multiplier based on Vedic Mathematics, proposed by Prabir Saha et al [7], takes 2.02 nsecs to compute an 8 x 8 query using 90 nm processes. The proposed design has used 180 nm technology libraries for implementing the multipliers. Considering the difference in technologies used for implementing the proposed algorithm and the Vedic, the proposed design is expected to be faster than the other. A similar result is believed to occurin the case of power consumption too.

IV. CONCLUSION

The new MAC unit design proposed here has significant advantages with regards to Propagation Delay (PD), Power Consumed and Area Occupied over other conventional multipliers including Booth recoded multipliers and array multipliers. Also the proposed design is found to be in termsof the parameters said above. More studies on it can be done to further improve the efficiency of the unit.

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